

FIGURE 1

PROVIDING AN INTEGRATED CIRCUIT
STRUCTURE HAVING A LAYER OF LOW K
CARBON-DOPED SILICON OXIDE DIELECTRIC
MATERIAL THEREON WITH VIAS ETCHED
THROUGH THE LAYER OF LOW K DIELECTRIC
MATERIAL USING A PHOTORESIST MASK OVER
THE LAYER OF LOW K DIELECTRIC MATERIAL

EXPOSING THE INTEGRATED CIRCUIT
STRUCTURE TO A PLASMA FORMED FROM ONE
OR MORE REDUCING AGENTS TO REMOVE AT
LEAST SOME OF THE RESIST MASK AND AT
LEAST SOME OF THE ETCH RESIDUES

EXPOSING THE INTEGRATED CIRCUIT STRUCTURE TO A DIRECTIONAL BEAM OF CHARGED PARTICLES FROM A PLASMA FORMED FROM ONE OR MORE OXIDIZING AGENTS TO REMOVE ANY REMAINING ETCH RESIDUES FROM BOTH FORMATION OF THE VIAS AND REMOVAL OF THE RESIST MASK